METHOD OF MANUFACTURING NON-VOLATILE SEMICONDUCTOR MEMORY ELEMENT AND METHOD OF MANUFACTURING NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

TECHNICAL FIELD

[0001] The present invention relates to a method of manufacturing a non-volatile memory element using a variable resistance element and a method of manufacturing a non-volatile memory device using a variable resistance element.

BACKGROUND ART

[0002] In recent years, with the advances in digital technologies employed for electronic apparatuses, large-capacity and non-volatile semiconductor memory devices for storing data, such as music, images, and information, have been actively developed. For example, a non-volatile semiconductor memory device using a ferroelectric as a capacitive element has already been used in many fields. In comparison with such a non-volatile semiconductor memory device using a ferroelectric capacitor, there is a non-volatile semiconductor memory device using a material that changes in resistance in response to the application of an electrical pulse and keeps the resulting state (referred to as the ReRAM hereafter). This ReRAM has received attention because consistency with a usual semiconductor process can be easily ensured (see Patent Literatures 1 and 2, for example).

[0003] With the aim of reducing the size and increasing the capacity for a memory element, a cross point ReRAM has been proposed. In the cross point ReRAM, a memory cell is formed at an intersection of an upper line and a lower line. This memory cell has a structure where a variable resistance layer is positioned between an upper electrode and a lower electrode. Moreover, each memory cell includes a diode inserted in series with the variable resistance layer. With this, when a resistance value of the variable resistance layer included in the memory cell is read, this memory cell can avoid influence (such as a leakage current) of another memory cell on a different row or column in a two-dimensional memory cell array.

[0004] FIG. **19** is a cross-section diagram showing, as a first example of the aforementioned cross point ReRAM, a non-volatile semiconductor memory device **1000** including a conventional variable resistance element (see Patent Literature 1). More specifically, FIG. **19** is a cross-section diagram of a memory cell **1280** along a bit-line direction, a bit line **1210**, and a word line **1220**. A variable resistance element **1260** includes: a variable resistance layer **1230** storing information according to an electrical-resistance change in response to an electrical stress; an upper electrode **1240**; and a lower electrode **1250**. Here, the variable resistance layer **1230** is positioned between the upper electrode **1240** and the lower electrode **1250**. A two-terminal nonlinear element **1270** having nonlinear current-voltage characteristics capable of passing current bidirectionally is formed on the variable resistance element **1260**. Thus, a series circuit of the variable resistance element **1260** and the nonlinear element **1270** form the memory cell **1280**. The nonlinear element **1270** is a two-terminal element, such as a diode, that has the nonlinear current-voltage characteristics whereby a current change is not consistent with a voltage change. Moreover, the bit line **1210** which is the upper line is electrically connected to the nonlinear element **1270**, and the word line **1220** which is the lower line is electrically connected to the lower electrode **1250** of the variable resistance element **1260**.

[0005] As a second example, Patent Literature 2 discloses a specific configuration and manufacturing method of a non-volatile semiconductor memory element into which a diode is inserted in series. The non-volatile semiconductor memory element disclosed in Patent Literature 2 includes: an electrode layer having a diode which is a non-ohmic characteristic element; at least one of an insulator layer or a semiconductor layer; and an interlayer insulating layer. Here, the electrode layer and the insulator or semiconductor layer are filled in a memory cell hole formed in the interlayer insulating layer. With this configuration, a front surface of the non-ohmic element can be formed smooth and flush with the interlayer insulating layer, and thus a favorable interfacial state of the non-ohmic element can be obtained. As a result, a decrease or variations in resistance to pressure due to, for example, electric field concentration can be prevented, and a current capacity can be increased.

CITATION LIST

Patent Literature

[PTL 1]

[0006] Japanese Unexamined Patent Application Publication No. 2006-203098

[PTL 2]

[0007] International Publication WO 2008/062688

SUMMARY OF INVENTION

Technical Problem

[0008] In the device disclosed in Patent Literature 1, the variable resistance element and the diode element are configured in a six-layer stacked structure including the bit line and the word line. When the word line is formed, the nonlinear element, the upper electrode, the variable resistance layer, and the lower electrode are patterned at one time in a direction of the word line. After this, when the bit line positioned as an uppermost layer is formed, the nonlinear element, the upper electrode, the variable resistance layer, and the lower electrode are patterned at one time in a direction of the bit line. As a result, a memory cell is formed only at an intersection of the bit line and the word line. However, using this manufacturing method, the stacked structure of the layers to be patterned becomes thick. Moreover, since plural element films comprising different materials are formed at one time, it is difficult to perform patterning by etching. In other words, this manufacturing method is not suited to miniaturizing a memory cell.

[0009] According to the method disclosed in Patent Literature 2, a part of an MIM non-ohmic element is filled in a memory plug. This filling process requires: a process of forming a concave part by eliminating the variable resistance layer formed outside the memory cell hole, by the chemical mechanical polishing (CMP) method and by eliminating a part of the variable resistance layer formed inside the memory cell hole by, for example, overpolishing; and a process of forming an electrode layer and eliminating the electrode layer formed outside the memory cell hole by the CMP process. This leads to a problem that the manufacturing method is